IN THE CLAIMS

Claims 1-21 (Cancelled).

22. (New) A capacitor, comprising:

a first node that receives a signal;

a first transistor comprising a gate node and at least one other node, the at least one other node being coupled to receive the signal from the first node; and

a second transistor comprising a gate node and at least one other node, the gate node of the second transistor being coupled to receive the signal from the gate node of the first transistor.

23. (New) The capacitor according to claim 22, wherein at least one of the first transistor and the second transistor comprises a metal-oxide-semiconductor (MOS) transistor.

24. (New) The capacitor according to claim 22, wherein the capacitor is a floating capacitor.

25. (New) The capacitor according to claim 22, further comprising:

a resistor coupled to the gate node of the first transistor and to the gate node of the second transistor.

26. (New) The capacitor according to claim 22, wherein the at least one other node of the first transistor comprises a first transistor node and a second transistor node, the first transistor node being coupled to the second transistor node and to the first node.

27. (New) The capacitor according to claim 22, further comprising:

a second node coupled to receive the signal from the at least one other node of the second transistor.

28. (New) The capacitor according to claim 27, wherein the first transistor and the second transistor provide a capacitance between the first node and the second node.

29. (New) The capacitor according to claim 27, wherein the at least one other node of the second transistor comprises a first transistor node and a second transistor node, the first transistor node being coupled to the second transistor node and to the second node.

30. (New) The capacitor according to claim 22, further comprising:

a bias source coupled to the gate node of the first transistor and to the gate node of the second transistor.

31. (New) A capacitor, comprising:

a first transistor comprising a first node, a second node and a third node, the first node being coupled to the second node; and

a second transistor comprising a fourth node, a fifth node and a sixth node, the fourth node being coupled to the fifth node, the sixth node being coupled to the third node,

wherein the first transistor and the second transistor provide a capacitance between the first node and the fourth node.

32. (New) The capacitor according to claim 31, wherein at least one of the first transistor and the second transistor comprises a metal-insulator-semiconductor transistor.

33. (New) The capacitor according to claim 31, wherein the capacitor is a floating capacitor.

34. (New) The capacitor according to claim 31,

wherein the first node or the fourth node comprises a drain node,

wherein the second node or the fifth node comprises a source node, and

wherein the third node or the sixth node comprises a gate node.

35. (New) The capacitor according to claim 31, further comprising:

a bias source coupled to the third node and to the sixth node via a bias resistor.

36. (New) The capacitor according to claim 31, further comprising:

a first signal node coupled to the first node and to the second node; and

a second signal node coupled to the fourth node and to the fifth node.

37. (New) The capacitor according to claim 36, wherein the first signal node and the second signal node provide the capacitance.

38. (New) The capacitor according to claim 36, wherein the signal passes from the first signal node to the second signal node via the first transistor and the second transistor.

39. (New) A method for providing a capacitance, comprising:

receiving a signal at a non-gate node of a first transistor;

sending the signal, received by the first transistor, from a gate node of the first transistor to a gate node of a second transistor; and

sending the signal, received by the second transistor, to a non-gate node of the second transistor.

40. (New) The method according to claim 39, wherein at least one of the first transistor and the second transistor comprises a metal-insulator-semiconductor transistor.

41. (New) The method according to claim 40, wherein the metal-insulator-semiconductor transistor comprises a MOS transistor.

42. (New) The method according to claim 39, wherein the capacitance is a floating capacitance.

43. (New) The method according to claim 39, wherein the first transistor comprises a second non-gate node, the second non-gate node being coupled to the non-gate node of the first transistor.

44. (New) An integrated circuit, comprising:

a first node that receives a signal;

a first transistor comprising a gate node and at least one other node, the at least one other node being coupled to receive the signal from the first node; and

a second transistor comprising a gate node and at least one other node, the gate node of the second transistor being coupled to receive the signal from the gate node of the first transistor.

45. (New) The integrated circuit according to claim 44, wherein at least one of the first transistor and the second transistor comprises a metal-oxide-semiconductor (MOS) transistor.

46. (New) The integrated circuit according to claim 44, wherein the capacitor is a floating capacitor.

47. (New) The integrated circuit according to claim 44, wherein the at least one other node of the first transistor comprises a first transistor node and a second transistor node, the first transistor node being coupled to the second transistor node and to the first node.

48. (New) The integrated circuit according to claim 44, further comprising:

a second node coupled to receive the signal from the at least one other node of the second transistor.

49. (New) The integrated circuit according to claim 48, wherein the first transistor and the second transistor provide a capacitance between the first node and the second node.

50. (New) The integrated circuit according to claim 44, wherein the at least one other node of the second transistor comprises a first transistor node and a second transistor node, the first transistor node being coupled to the second transistor node and to the second node.

51. (New) The integrated circuit according to claim 44, further comprising:

a bias source coupled to the gate node of the first transistor and to the gate node of the second transistor.

52. (New) An integrated circuit, comprising:

a first transistor comprising a first node, a second node and a third node, the first node being coupled to the second node; and

a second transistor comprising a fourth node, a fifth node and a sixth node, the fourth node being coupled to the fifth node, the sixth node being coupled to the third node,

wherein the first transistor and the second transistor provide a capacitance between the first node and the fourth node.

53. (New) The integrated circuit according to claim 52, wherein at least one of the first transistor and the second transistor comprises a metal-insulator-semiconductor transistor.

54. (New) The integrated circuit according to claim 52, wherein the capacitor is a floating capacitor.

55. (New) The integrated circuit according to claim 52,

wherein the first node or the fourth node comprises a drain node,

wherein the second node or the fifth node comprises a source node and

wherein the third node or the sixth node comprises a gate node.

56. (New) The integrated circuit according to claim 52, further comprising:

a bias source coupled to the third node via a bias resistor and to the sixth node via the bias resistor.

57. (New) The integrated circuit according to claim 52, further comprising:

a first signal node coupled to the first node and to the second node; and

a second signal node coupled to the fourth node and to the fifth node.

58. (New) The integrated circuit according to claim 57, wherein the capacitance is formed between the first signal node and the second signal node.

59. (New) A tunable capacitor array, comprising:

a plurality of capacitors, each capacitor comprising:

a first node that receives a signal,

a first transistor comprising a gate node and at least one other node, the at least one other node being coupled to receive the signal from the first node, and

a second transistor comprising a gate node and at least one other node, the gate node of the second transistor being coupled to receive the signal from the gate node of the first transistor; and

a plurality of switches, each switch being coupled to a corresponding capacitor of the plurality of capacitors.

60. (New) The tunable capacitor array according to claim 59, wherein at least one of the first transistor and the second transistor comprises a metal-oxide-semiconductor (MOS) transistor.

61. (New) The tunable capacitor array according to claim 59, wherein the capacitor is a floating capacitor.

62. (New) The tunable capacitor array according to claim 59, wherein the at least one other node of the first transistor comprises a first transistor node and a second transistor node, the first transistor node being coupled to the second transistor node and to the first node.

63. (New) The tunable capacitor array according to claim 59, further comprising:

a second node coupled to receive the signal from the at least one other node of the second transistor.

64. (New) The capacitor according to claim 63, wherein the first transistor and the second transistor provide a capacitance between the first node and the second node.

65. (New) The tunable capacitor array according to claim 63, wherein the at least one other node of the second transistor comprises a first transistor node and a second transistor node, the first transistor node being coupled to the second transistor node and to the second node.

66. (New) The tunable capacitor array according to claim 59, further comprising:

a bias source coupled to the gate node of the first transistor and to the gate node of the second transistor.

67. (New) A tunable capacitor array, comprising:

a plurality of capacitors, each capacitor comprising:

a first transistor comprising a first node, a second node and a third node, the first node being coupled to the second node, and

a second transistor comprising a fourth node, a fifth node and a sixth node, the fourth node being coupled to the fifth node, the sixth node being coupled to the third node,

wherein the first transistor and the second transistor form a capacitance between the first node and the fourth node; and

a plurality of switches, each switch being coupled to a corresponding capacitor of the plurality of capacitors.

68. (New) The tunable capacitor array according to claim 67, wherein at least one of the first transistor and the second transistor comprises a metal-insulator-semiconductor transistor.

69. (New) The tunable capacitor array according to claim 67, wherein the capacitor is a floating capacitor.

70. (New) The tunable capacitor array according to claim 67,

wherein the first node or the fourth node comprises a drain node,

wherein the second node or the fifth node comprises a source node, and

wherein the third node or the sixth node comprises a gate node.

71. (New) The tunable capacitor array according to claim 67, further comprising:

a bias source coupled to the third node via a bias resistor and to the sixth node via the bias resistor.

72. (New) The tunable capacitor array according to claim 67, further comprising:

a first signal node coupled to the first node and to the second node; and

a second signal node coupled to the fourth node and to the fifth node.

73. (New) The tunable capacitor array according to claim 72, wherein the capacitance is formed between the first signal node and the second signal node.